Page 27, replace last paragraph spanning pages 27 and 28 as follows:

--As described above, by disposing the upper floating gate 24 larger in area size than the lower floating gate 4 on the lower floating gate 4 which is oppositely disposed from the control gate 11 through the floating gate covering insulation film 16, it is possible for the lower floating gate 4 to increase in effect its surface area oppositely disposed from the control gate 11. Consequently, it is also possible to increase a capacitance between the lower floating gate 4 and the control gate 11. Potential of the lower floating gate 4 and the control gate 11 and a capacitance between the lower floating gate 4 and the semiconductor substrate 1. Consequently, it is possible to increase in potential the lower floating gate 4 by increasing the capacitance between the control gate 11 and the lower floating gate 4. As a result, in the second embodiment of the nonvolatile semiconductor memory device of the present invention having the above construction, it is possible to decrease a voltage applied to the control gate 11, which permits a write voltage to be decreased.--

8020-1002-1 Amendment

REMARKS

Claims 1-9 are pending in the present application.